In the claims:

Please substitute the following full listing of claims with their current status for the claims as originally submitted or most recently amended. The following amendments correct the amendments filed June 20, 2005, which were not entered and present additional amendatory language (referenced to the amendments filed December 10, 2004). The amendments presented June 20, 2005 should be disregarded. The remarks included in that response are repeated below for the convenience of the Examiner.

1. (Currently Amended) An integrated circuit including

a patterned copper layer,.

a patterned aluminum layer,

an opening in a layer of material, said opening extending between a location on said patterned copper layer and a location on said patterned aluminum layer,

a multi-layer barrier liner in said opening and having a thickness, said barrier liner extending between said patterned aluminum layer and said patterned copper layer at said location on said patterned copper layer and across said copper layer to cover a bottom of said opening, said multi-layer barrier layer including at least a first layer being of a material which is conductive and ~~has~~ having adhesion to copper and tungsten comparable to that of tantalum or tantalum nitride or titanium nitride and ~~resists~~ resisting interdiffusion of copper and tungsten and a second layer formed on said first layer and being of a material which assists in the formation of a stud during deposition of tungsten on which tungsten can be deposited, one or both of said first and second layers forming a conductive barrier to process materials which are reactive with copper, and

a stud connection formed of tungsten and located within said barrier liner.

2. (Original) An integrated circuit as recited in claim 1 wherein said liner comprises

a layer of tantalum nitride, and

a layer of PVD tungsten.

3. (Previously Presented) An integrated circuit as recited in claim 1 wherein said liner comprises

a layer of tantalum nitride,

a layer of titanium nitride, and

a layer of titanium nitride or PVD tungsten.

4. (Cancelled)

5. (Original) An integrated circuit as recited in claim 1 wherein said patterned aluminum layer includes a layer of at least one of titanium and titanium nitride.

6. (Original) An integrated circuit as recited in claim 2 wherein said patterned aluminum layer includes a layer of at least one of titanium and titanium nitride.

7. (Original) An integrated circuit as recited in claim 3 wherein said patterned aluminum layer includes a layer of at least one of titanium and titanium nitride.

8. (Cancelled)

9. (Original) An integrated circuit as recited in claim 1, further including a covering layer.

10. (Original) An integrated circuit as recited in claim 9 wherein said covering layer includes a layer of silane-based high density plasma oxide.

11. - 16. (Canceled)